then accepts and decodes the digital signal producing data. The decoder may be a trellis decoder, and embodiments may incorporate a decision feedback equalizer.

Additionally methods corresponding to functions performed by the apparatuses may form embodiments of the invention.

Page 5, paragraph 4, line 32 through page 6, line 10, replace the paragraph with the following rewritten paragraph:

Figure 3 is a block diagram illustrating the fiber optic transmitter 200 according to an embodiment of the current invention. Detail of the transmitter 200 is illustrated in Figure 3. The trellis encoder 323 accepts a group of R bits from the data source 202. The trellis encoder 305 is a rate M/(M+1) convolutional coder of the R bits which are input to the rate M/(M+1) encoder. R-M bits will be unencoded and M bits will be encoded. The output of the convolutional coder 305 comprises (M+1) bits. The R-M unencoded bits and the M + 1 coded bits, which are output from the convolutional coder 305, are provided to a subset mapper 307. The subset mapper 307 maps the received bits into a series of multilevel symbols 309, for example, PAM 5 symbols. The combination of convolutional coder 305 and the R-M unencoded bits comprises a trellis encoder 323. The pulse amplitude modulated signals A_1 through A_N have 5 levels, but may have any number of amplitude levels, but are not limited to such. Any number of amplitude levels may be chosen depending on the pulse amplitude modulation scheme chosen.

On page 6, paragraph 3, line 20, replace the paragraph with the following rewritten paragraph:

In Figure 3 multilevel symbols 309 are provided to a Tomlinson precoder. The exemplary system illustrated in Figure 3 is a 10 gigabit per second (Gb/s) transmission system implemented using a five level pulse amplitude modulation - 5 level (PAM-5) transmission

scheme. The baud rate necessary to achieve a 10 Gb/s transmission is reduced to five gigabaud because each PAM-5 symbol can represent two bits.

Page 8, paragraph 1, line 11, replace the paragraph with the following rewritten paragraph:

Difficulties can be encountered because at frequencies where the channel exhibits significant attenuation, the precoder will require significant gain to compensate for the attenuation. At such frequencies due to the increased gain, the precoder may become unstable. In order to stabilize the precoder and to limit the amplitude of the signal out of the precoder, a signal V_n, represented by arrow 403 is added to the summation unit 405A. $V_n = K_n \times M$ where M is the number of levels being transmitted on the channel. In the present PAM-5 embodiment, M has a value of 5. The output signal of the precoder, V_n, is computed and if the signal exceeds certain limits then V_n is subtracted from the signal Y_n. K_n is the smallest integer that returns the output Y_n back into the desired range. M is essentially the maximum allowable range of the output of the precoder. Depending on the value of Y_n there is a integer value K_n that will bring the output of the precoder back within the range M. This is the basis of Tomlinson Harashima Precoding (THP). In other words, the THP inverse channel characteristic filtering then modifies the input to the summation unit by adding an integral multiple of M (i.e., V_n) which makes the output bounded to the input. The output of the channel sees a quantity equal to X_n plus V_n. In other words, the number of levels appearing at the receiver has been expanded. Accordingly, the slicer in the receiver must be able to distinguish $X_n + V_n$ levels instead of just being able to distinguish X_n levels. One consequence of such equalization is the increase of the number of levels in the constellation at the receiver. Therefore, to recover the original PAM-5 levels in the receiver a wrap-around scheme, such

that the excess levels are wrapped around into the original PAM-5 levels. Such a wrap around is illustrated in Figure 4A.

Page 11, paragraph 1, line 5, replace the paragraph with the following rewritten paragraph:

The analog to digital converters (A/D) 509 are timed by a clock provided by the timing recovery circuit 515. Each A/D converter, however, receives its own phase of the clock in order to sample successive values using successive A/D converters. Because the values received by the A/D converters are sampled using a clock having different phases, retiming of the signals is necessary in order to create a synchronized parallel value. The retiming of the A/D samples takes place in retiming block 511. Retiming block 511 essentially comprises a clocked register circuit or equivalent. By interleaving N A/D converters in the analog to digital block 509, the clock rate of each individual converter can be reduced by a factor of N (over the use of a single converter). Without the interleaving of analog to digital converters 509 it may be difficult or impossible to fabricate an analog to digital converter, which could sample the input at a high enough rate, in order not to lose any successive values in the input data stream. By interleaving the A/D converters the necessity of using very high speed circuit technologies, such as gallium arsenide or indium phosphide may be avoided.

Page 11, paragraph 3, line 25, replace the paragraph with the following rewritten paragraph:

The output of the fine AGC block 513 is coupled into K-way interleaved L-dimensional trellis decoder. The number K of trellis decoders will vary depending on a variety of implementation details. The N-dimensional trellis decoder 519 decodes the symbols accepted from the fine AGC module 513 and converts them into digital data values.